We Claim:

1. An integrated circuit, comprising:

a reconfigurable interconnect portion;

a data processing portion coupled to the reconfigurable interconnect portion, the data processing portion configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion; and

a storage unit coupled to the data processing portion, the storage unit including a configuration bit look-up table.

2. The integrated circuit of claim 1, wherein the integrated circuit includes a second reconfigurable interconnect portion, and configuration bit look-up table is configured to allow the data processing portion to extract a first set of configuration bits representing the bit pattern and to extract a second set of configuration bits representing a second bit pattern to load a second configuration of the second reconfigurable interconnect portion, wherein the second set is a subset of the first set.

3. The integrated circuit of claim 1, wherein the reconfigurable interconnect portion comprises a switching matrix.

4. The integrated circuit of claim 1, wherein reconfigurable interconnect portion comprises a multiplexor.

5. The integrated circuit of claim 3, wherein the switching matrix includes a control signal input configured to select between two inputs to connect to an output.

6. The integrated circuit of claim 1, wherein the reconfigurable interconnect portion comprises a pair of transistors.

7. The integrated circuit of claim 1, wherein the reconfigurable interconnect portion comprises a plurality of memory elements, each memory element connected to at least one switch of the reconfigurable interconnect portion.

8. The integrated circuit of claim 1, wherein the bit pattern is derived from the configuration bit look-up table.

9. The integrated circuit of claim 1, wherein the configuration bit look-up table comprises a plurality of rows of configuration bits.

10. The integrated circuit of claim 9, wherein the storage unit is coupled to the data processing portion by a plurality of address lines for accessing the rows of configuration bits stored within the storage unit.

11. The integrated circuit of claim 10, wherein the storage unit further comprises programming instructions configured for accessing the configuration bit look-up table, wherein the programming instructions are further configured for extracting a subset of configuration bits from the configuration bit look-up table.

12. The integrated circuit of claim 1, wherein the data processing portion is configured to map a first input of the reconfigurable interconnect portion to a first output of the reconfigurable interconnect portion in response to a first command.

13. The integrated circuit of claim 12, wherein the data processing portion is configured to map a second input of the reconfigurable interconnect portion to a second output of the reconfigurable interconnect portion in response to the first command.

14. The integrated circuit of claim 12, wherein the data processing portion is configured to map a second input of the reconfigurable interconnect portion to a second output of the reconfigurable interconnect portion in response to a second command.

15. The integrated circuit of claim 12, further comprising a second reconfigurable interconnect portion, and wherein the data processing portion is configured to map a first input of the second reconfigurable interconnect portion to a first output of the second reconfigurable interconnect portion in response to a second command.

16. An emulation system comprising:

a plurality of emulation boards;

a plurality of interconnect boards interconnecting the plurality of emulation boards, wherein each of the plurality of interconnect boards has a reconfigurable interconnect portion and a data processing portion coupled to the reconfigurable interconnect portion; and

a storage unit coupled to the data processing portion,

wherein, for each interconnect board, the data processing portion is configured to provide a bit pattern to the respective reconfigurable interconnect portion to load a configuration of the respective reconfigurable interconnect portion, and

wherein the storage unit includes a configuration bit look-up table.

17. The emulation system of claim 16, wherein the configuration bit look-up table is configured to allow each data processing portion of the plurality of interconnect boards to extract a set of configuration bits representing the bit pattern to the respective interconnect portion, wherein at least one set of configuration bits is a subset of another set of configuration bits.

18. The emulation system of claim 16, wherein the reconfigurable interconnect portion comprises a switching matrix.

19. The emulation system of claim 16, wherein the reconfigurable interconnect portion comprises a multiplexor.

20. The emulation system of claim 16, wherein the reconfigurable interconnect portion comprises a pair of transistors.

21. The emulation system of claim 16, wherein the reconfigurable interconnect portion comprises at least one memory element.

22. The emulation system of claim 16, wherein the bit-pattern is derived from the configuration bit look-up table.

23. The emulation system of claim 16, wherein the data processing portion is configured to map an input of the reconfigurable interconnect portion to an output of the reconfigurable interconnect portion in response to a command.

24. The emulation system of claim 16, wherein each of the plurality of interconnect boards has an integrated circuit, wherein each integrated circuit includes the reconfigurable interconnect portion and the data processing portion of the respective interconnect portion.

25. The emulation system of claim 16, wherein the storage unit is located in a workstation external to the plurality of emulation boards and the plurality of interconnect boards.

26. The emulation system of claim 16, wherein the configuration bit look-up table is at least partially embodied as software written onto a computer-readable medium.

27. A method for configuring a reconfigurable interconnect portion in an emulation system, the method comprising steps of:

receiving a command to configure a reconfigurable interconnect portion, thereby configuring a set of switches of the reconfigurable interconnect portion;

determining configuration bits to configure the reconfigurable interconnect portion; and

providing the determined configuration bits to the reconfigurable interconnect portion to configure the set of switches of the reconfigurable interconnect portion,

wherein the configuration bits are derived from a configuration bit look-up table.

28. The method of claim 27, wherein the command identifies the reconfigurable interconnect portion to be configured.

29. The method of claim 27, wherein the command includes information to configure a second set of switches of the reconfigurable interconnect portion.

30. The method of claim 29, wherein the determined configuration bits further configure the second set of switches.

31. The method of claim 27, wherein said step of determining comprises steps of:

accessing the configuration bit look-up table; and

extracting a subset of configuration bits.

32. The method of claim 27, wherein the step of providing comprises a step of:

mapping a first input of the reconfigurable interconnect portion to a first output of the reconfigurable interconnect portion responsive to the command.

33. The method of claim 32, wherein the step of providing further comprises a step of:

mapping a second input of the reconfigurable interconnect portion to a second output of the reconfigurable interconnect portion responsive to the command.

34. The method of claim 32, further comprising a step of receiving a second command to configure the reconfigurable interconnect portion,

wherein the step of providing further comprises a step of:

mapping a second input of the reconfigurable interconnect portion to a second output of the reconfigurable interconnect portion responsive to the second command.

35. An integrated circuit comprising a reconfigurable interconnect portion and a storage unit coupled to the reconfigurable interconnect portion, wherein the storage unit stores a look-up table for use in configuring the reconfigurable interconnect portion.

36. An integrated circuit, comprising:

a reconfigurable interconnect portion;

a data processing portion coupled to the reconfigurable interconnect portion, the data processing portion configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion; and

a storage unit coupled to the data processing portion, the storage unit including a look-up table,

wherein the look-up table is configured to allow the data processing portion to extract a first set of bits representing the bit pattern and to extract a second set of bits representing a second bit pattern to load a second configuration of a second reconfigurable interconnect portion, wherein the second set is a subset of the first set.

37. A method of configuring a reconfigurable interconnect portion, comprising steps of:

determining configuration bits to configure the reconfigurable interconnect portion;

accessing a configuration bit-look up table;

extracting a set of configuration bits representing the bit pattern from the configuration bit look-up table; and

providing the set of configuration bits representing the requested bit pattern.

38. A method of configuring a reconfigurable interconnect portion of a circuit, comprising steps of:

receiving a set of configuration bits representing the requested bit pattern; and

configuring a reconfigurable interconnect portion based on the received configuration bits,

wherein the configuration bits are derived from a configuration bit look-up table.